

Jieming Yin

Office: Packard Lab Room 402A,
19 Memorial Drive West,
Bethlehem, PA 18015

Email: yin@lehigh.edu
Web: <http://jiemingyin.github.io/>

EDUCATION

University of Minnesota, Twin Cities, Minneapolis, MN
Ph.D. in Computer Science, 2015
Dissertation: Time-Division-Multiplexing Based Hybrid-Switched NoC for Heterogeneous Multicore Systems
Advisor: Antonia Zhai

Harbin Institute of Technology, Harbin, China
B.Eng. in Electrical Engineering, 2008
Thesis: Point-to-point Scalar Operand Networks for Clustered Superscalar Processor

EMPLOYMENT

Lehigh University, Bethlehem, PA Aug. 2020 - Present
Assistant Professor, Department of Electrical and Computer Engineering

AMD Research, Bellevue, WA Dec. 2016 - Aug. 2020
Member of Technical Staff Silicon Design Engineer

AMD Research, Bellevue, WA Mar. 2015 - Dec. 2016
Postdoc Researcher

PUBLICATIONS

Refereed Conference Publications

- Yuan Zhou, Hanyu Wang, **Jieming Yin**, Zhiru Zhang. *Distilling Arbitration Logic from Traces using Machine Learning: A Case Study on NoC*. 58th Annual Design Automation Conference (DAC), Virtual Conference, July, 2021.
- Subhash Sethumurugan, **Jieming Yin**, John Sartori. *Designing a Cost-Effective Cache Replacement Policy using Machine Learning*. 27th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Virtual Conference, February, 2021.
- **Jieming Yin**, Antonia Zhai. *In-Network Memory Access Ordering for Heterogeneous Multicore Systems*. 14th IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Virtual Conference, September, 2020. (**Best Paper Award**)
- Srikant Bharadwaj, **Jieming Yin**, Bradford M. Beckmann, Tushar Krishna. *Kite: A Family of Heterogeneous Interposer Topologies Enabled via Accurate Interconnect Modeling*. 57th Annual Design Automation Conference (DAC), Virtual Conference, July, 2020.
- **Jieming Yin**, Subhash Sethumurugan, Yasuko Eckert, Alan Smith, Chintan Patel, Eric Morton, Mark Oskin, Natalie Enright Jerger, Gabriel H. Loh. *Experiences with ML-Driven Design: A NoC Case Study*. 26th IEEE International Symposium on High-Performance Computer Architecture (HPCA), San Diego, CA, February 2020.
- Shuai Che, **Jieming Yin**. *Northup: Divide-and-Conquer Programming in Systems with Heterogeneous Memories and Processors*. 33rd IEEE International Parallel & Distributed Processing Symposium (IPDPS), Rio de Janeiro, Brazil, May 2019.
- **Jieming Yin**, Zhifeng Lin, Onur Kayiran, Matthew Poremba, Muhammad Shoaib Bin Altaf, Natalie Enright Jerger, Gabriel H. Loh. *Modular Routing Design for Chiplet-based Systems*. 45th International Symposium on Computer Architecture (ISCA), Los Angeles, CA, June 2018. (**Featured in IEEE Spectrum**)
- Anthony Gutierrez, Bradford Beckmann, Alexandru Dutu, Joseph Gross, John Kalamantianos, Onur Kayiran, Michael LeBeane, Matthew Poremba, Brandon Potter, Sooraj Puthoor, Mark Wyse, **Jieming Yin**, Akshay Jain, Tim Rogers, Xianwei Zhang, Matt Sinclair. *Lost*

in Abstraction: Pitfalls of Analyzing GPUs at the Intermediate Language Level. 24th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Vienna, Austria, February 2018.

- Matthew Poremba, Itir Akgun, **Jieming Yin**, Onur Kayiran, Yuan Xie, Gabriel H. Loh. *There and Back Again: Optimizing the Interconnect in Networks of Memory Cubes*. 44th International Symposium on Computer Architecture (ISCA), Toronto, CA, June 2017.
- **Jieming Yin**, Onur Kayiran, Matthew Poremba, Natalie Enright Jerger, Gabriel H. Loh. *Efficient Synthetic Traffic Models for Large, Complex SoCs*. 22nd International Symposium on High Performance Computer Architecture (HPCA), Barcelona, Spain, March 2016.
- **Jieming Yin**, Pingqiang Zhou, Sachin S. Sapatnekar, Antonia Zhai. *Energy-Efficient Time-Division Multiplexed Hybrid-Switched NoC for Heterogeneous Multicore Systems*. 28th IEEE International Parallel & Distributed Processing Symposium (IPDPS), Phoenix, Arizona, USA, May 2014.
- **Jieming Yin**, Pingqiang Zhou, Anup P. Holej, Sachin S. Sapatnekar, Antonia Zhai. *Energy Efficient Non-Minimal Path On-chip Interconnection Network for Heterogeneous Multicore Systems*. International Symposium on Low Power Electronics and Design (ISLPED), Redondo Beach, USA, August 2012.
- Pingqiang Zhou, **Jieming Yin**, Antonia Zhai, Sachin S. Sapatnekar. *NoC Frequency Scaling with Flexible-Pipeline Routers*. International Symposium on Low Power Electronics and Design (ISLPED), Fukuoka, Japan, August 2011.
- Bing Yang, Zhigang Mao, **Jieming Yin**, Xiao Chen. *A Point to Point Inter-cluster Communication Network in Clustered Superscalar Processor*. International Conference on Solid-State and Integrated-Circuit Technology (ICSICT), Beijing, China, October 2008.

Refereed Journal Publications

- Xiangwei Cai, **Jieming Yin**, Pingqiang Zhou. *An orchestrated NoC prioritization mechanism for heterogeneous CPU-GPU systems*. Integration, Volume 65, March 2019.

Workshop and Technical Report

- **Jieming Yin**, Yasuko Eckert, Shuai Che, Mark Oskin, Gabriel H. Loh. *Toward More Efficient NoC Arbitration: A Deep Reinforcement Learning Approach*. The 1st International Workshop on AI-assisted Design for Architecture (AIDArc), Los Angeles, CA, June 2018.
- Pingqiang Zhou, **Jieming Yin**, Antonia Zhai, Sachin S. Sapatnekar. *NoC Design and Performance Optimization*. SRC TECHCON, 2011.

US Patent and Application

- US Patent 10,042,774. Shuai Che, **Jieming Yin**. *Method and apparatus for masking and transmitting data*. Granted Aug. 2018.
- US Patent 10,389,251. Wei Huang, Yasuko Eckert, Xudong An, Muhammad Shoaib Bin Altaf, **Jieming Yin**. *Setting operating points for circuits in an integrated circuit chip*. Granted Oct. 2018.
- US Patent 10,097,091. Wei Huang, Yasuko Eckert, Xudong An, Muhammad Shoaib Bin Altaf, **Jieming Yin**. *Setting operating points for circuits in an integrated circuit chip*. Granted Oct. 2018.
- US Patent 10,719,441. **Jieming Yin**, Yasuko Eckert, Matthew Poremba, Steven Raasch, Doug Hunt. *Using Predictions of Outcomes of Cache Memory Access Requests for Controlling Whether A Request Generator Sends Memory Access Requests To A Memory In Parallel With Cache Memory Access Requests*. Granted Jul. 2020.
- US Patent App 15/922,875. Shuai Che, **Jieming Yin**. *Reconfigurable prediction engine for general processor counting*. Filed Mar. 2018.

- US Patent App 15/948,795. Tony Gutierrez, Sergey Blagodurov, Scott Moe, Xianwei Zhang, **Jieming Yin**, Matt Sinclair. *Selecting a precision level for executing a workload in an electronic device*. Filed Apr. 2018.
- US Patent App 16/176,903. Shuai Che, **Jieming Yin**. *Architecture for deep Q-learning*. Filed Oct. 2018.
- US Patent App 16/224,739. Mohamed Ibrahim, Onur Kayiran, Yasuko Eckert, **Jieming Yin**. *A Mechanism for Dynamic Latency-Bandwidth Trade-off for Efficient Broadcasts/Multicasts*. Filed Dec. 2018.

AWARDS AND HONORS

- Best Paper Award, 14th IEEE/ACM International Symposium on Networks-on-Chip (NOCS), 2020

SCHOLARLY PRESENTATIONS

- *In-Network Memory Access Ordering for Heterogeneous Multicore Systems*. International Symposium on Networks-on-Chip (NOCS), Virtual Conference, Sep. 2020.
- *In-Package Interconnection Networks in the Era of Exascale and Beyond*. Seminar talk at College of William and Mary, Williamsburg, VA, Mar. 2020.
- *In-Package Interconnection Networks in the Era of Exascale and Beyond*. Seminar talk at Illinois Institute of Technology, Chicago, IL, Jan. 2020.
- *In-Package Interconnection Networks in the Era of Exascale and Beyond*. Seminar talk at Lehigh University, Bethlehem, PA, Jan. 2020.
- *In-Package Interconnection Networks in the Era of Exascale and Beyond*. Seminar talk at Virginia Tech, Blacksburg, VA, Jan. 2020.
- *Experiences with ML-Driven Design: A NoC Case Study*. International Symposium on High-Performance Computer Architecture (HPCA), San Diego, CA, Feb. 2020.
- *Exploiting Machine Learning Insights for NoC Design*. Presented to the Department of Energy (DOE), Bellevue, WA, Apr. 2019.
- *Better NoCs through Machine Learning*. Presented to the Department of Energy (DOE), Austin, TX, Sep. 2018.
- *Modular Routing Design for Chiplet-based Systems*. International Symposium on Computer Architecture (ISCA), Los Angeles, CA, Jun. 2018.
- *Toward More Efficient NoC Arbitration: A Deep Reinforcement Learning Approach*. International Workshop on AI-assisted Design for Architecture (AIDArc), Los Angeles, CA, Jun. 2018.
- *Designing Energy-Efficient NoCs for Heterogeneous Multicore Systems*. Invited talk at Nvidia, Santa Clara, CA, Feb. 2015.
- *Energy-Efficient Time-Division Multiplexed Hybrid-Switched NoC for Heterogeneous Multicore Systems*. 28th IEEE International Parallel & Distributed Processing Symposium (IPDPS), Phoenix, AZ, May. 2014.
- *Energy Efficient Non-Minimal Path On-chip Interconnection Network for Heterogeneous Multicore Systems*. International Symposium on Low Power Electronics and Design (ISLPED), Redondo Beach, CA, Jul. 2012.
- *NoC Frequency Scaling with Flexible-Pipeline Routers*. International Symposium on Low Power Electronics and Design (ISLPED), Fukuoka, Japan, Aug. 2011.

**TEACHING AND
RESEARCH
ADVISING**

Courses Taught

- **ECE 201 - Computer Architecture**
Spring 2021
- **ECE 450 - Interconnection Networks for Many-core Architectures**
Fall 2020

Student Advising

- Subhash Sethumurugan, PhD student, University of Minnesota, Twin Cities, 2018-present.
Project: Exploiting Machine Learning Insights for Cache Replacement Policy
- Zhifeng Lin, Master student, University of Southern California, 2016-2017.
Project: Exploring QoS in Interposer-based Systems

SERVICE

Conference Organizing Committee

- Publicity Chair, IEEE/ACM International Symposium on Networks-on-Chip (NOCS), 2021.
- Finance Chair, IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2019.
- Submissions Chair, IEEE International Symposium on Workload Characterization (IISWC), 2017.

Conference Technical Program Committee

- ACM International Conference on Supercomputing (ICS), 2021.
- Design Automation Conference (DAC), 2019-2021.
- (External Review Committee) International Conference on Parallel Architectures and Compilation Techniques (PACT), 2020.
- IEEE/ACM International Symposium on Networks-on-Chip (NOCS), 2019-2020.
- IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2019-2020.
- Workshop on General Purpose Processing Using GPU (GPGPU), 2020.
- IEEE International Symposium on Workload Characterization (IISWC), 2017.
- IEEE International Conference on High Performance Computing, Data, and Analytics (HiPC), 2016.

Journal Editor

- Guest Editor, Journal of Signal Processing Systems special issue on Application-specific Systems, Architectures and Processors, 2020.

Journal Reviewer

- ACM Transactions on Architecture and Code Optimization (TACO)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on Computers Special Issue on Communications for Many-Core Processors and Accelerators
- IEEE Transactions on Parallel and Distributed Systems (TPDS)
- IEEE Computer Architecture Letters (CAL)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- Journal of Systems Architecture (JAS)
- EURASIP Journal on Embedded Systems